What is claimed is:

1. A circuit for compensating for a skew between an output data signal and an external clock signal, the circuit comprising:

a phase detector (PD) for detecting a phase difference between the output data signal and the external clock signal and for generating an up signal or a down signal depending on the detected phase difference;

an up-down counter enabled by a calibration signal that directs a compensation of the skew, for generating an offset code in response to the up signal or the down signal;

a delay locked loop (DLL) circuit for receiving the offset code in response to the calibration signal and for generating first and second clock signals having first and second phase differences, respectively, from the external clock signal; and

an output driver (OD) for generating the output data signal in response to the first clock signal.

2. The circuit of claim 1, wherein the first and second phase differences are 0° and 90°, respectively.

3. The circuit of claim 2, wherein the DLL circuit comprises:

a PD for detecting a phase difference between the external clock signal and the second clock signal;

a state machine for controlling a delay in response to the phase difference detected by the PD of the DLL;

a first adder for receiving an offset code from the up-down counter in response to the calibration signal;

a second adder for receiving the output of the first adder and the output of the state machine;

a first phase mixer for generating the first clock signal in response to the output of the second adder; and

a second phase mixer for generating the second clock signal in response to the output of the state machine.

4. A memory device for compensating for a skew between an output data signal and an external clock signal, the memory device comprising:

a phase detector (PD) for detecting a phase difference between the output data signal and the external clock signal and for generating an up signal or a down signal depending on the detected phase difference;

an up-down counter enabled by a calibration signal that directs a compensation of the skew, for generating an offset code in response to the up signal or the down signal;

a delay locked loop (DLL) circuit for receiving the offset code in response to the calibration signal and for generating first and second clock signals having first and second phase differences, respectively, from the external clock signal;

an output driver (OD) toggled by the first clock signal to generate the output data signal in response to the calibration signal; and

an OD replicator for receiving the second clock signal and for sending the second clock signal to the DLL circuit.

5. The memory device of claim 4, wherein the first and second phase differences are 0° and 90°, respectively.

6. The memory device of claim 4, further comprising:

a first path including a transmission line via which the first clock signal travels;

a second path including a transmission line via which the second clock signal travels, wherein the second path controls a duty of the second clock signal; and

a third path including a transmission line, wherein the third path controls a duty of the first clock signal.

7. The memory device of claim 4, further comprising:

a multiplexer (MUX) for controlling the OD in response to the first clock signal, the calibration signal and an internal data signal.

8. The memory device of claim 4, wherein the DLL circuit comprises:

a phase detector (PD) for receiving the external clock signal and the output of the OD replicator and for detecting a phase difference between the external clock signal and the output of the OD replicator;

a state machine for controlling a delay in response to the phase difference detected by the PD of the DLL;

a first adder for receiving an offset code from the up-down counter in response to the calibration signal;

a second adder for receiving the output of the first adder and the output of the state machine;

a first phase mixer for generating the first clock signal in response to the output of the second adder; and

a second phase mixer for generating the second clock signal in response to the output of the state machine.

9. The memory device of claim 8, wherein the offset code is provided to the first adder so that a centering error between the external clock signal and the output data signal are reflected in the first clock signal.

10. A method of compensating for a skew between an output data signal and an external clock signal, the method comprising:

detecting a phase difference between the output data signal and the external clock signal and generating an up signal or a down signal depending on the detected phase difference;

generating an offset code in response to the up signal or the down signal and a calibration signal that directs a compensation of the skew;

generating first and second clock signals having first and second phase differences, respectively, from the external clock signal, by using a delay locked loop (DLL) circuit;

detecting a phase difference between the external clock signal and the second clock signal;

controlling a delay in response to the detected phase difference; and

receiving the offset code in response to the calibration signal and generating the first and second clock signals.

11. The method of claim 10, wherein the first and second phase differences are 0° and 90°, respectively.

12. A method of compensating for a skew between an output data signal and an external clock signal using a memory device, the method comprising:

generating first and second clock signals having first and second phase differences, respectively, from the external clock signal;

detecting a phase difference between the output data signal and the external clock signal and generating an up signal or a down signal depending on the detected phase difference;

activating a calibration signal that directs a compensation of the skew and generating an offset code in response to the up or down signal;

receiving the offset code in response to the activated calibration signal and aligning edges of the first clock signal with edges of the output data signal, which is toggled by the first clock signal;

resetting the offset code in response to the inactivation of the calibration signal; and

aligning edges of the external clock signal with the middle points of the output data signal in response to the resetting of the offset code.

13. The method of claim 12, wherein the first and second phase differences are 0° and 90°, respectively.

14. The method of claim 12, wherein the memory device comprises:

a phase detector (PD); and

an up-down counter, wherein the PD and the up-down counter generate the offset code, wherein the offset code corresponds to the clock skew.